

Thank you for taking the Week 12 : Assignment 12.

Course outline

How does an NPTEL online course work?

Week 0

Week 1

Week 2

Week 3

Week 4

Week 5

Week 6

Week 7

Week 8

Week 12 : Assignment 12

Your last recorded submission was on 2021-10-20, 14:38 IST

Due date: 2021-10-20, 23:59 IST.

1) In MIPS32 floating-point extension, for double-precision operations the register pair <F14, F15> is referred as:

1 point

- a. F15
- b. F14
- c. F13
- d. F12
- e. None of these

- a.
- b.
- c.
- d.
- e.

Week 9

Week 10

Week 11

Week 12

Lecture 59: MULTICYCLE OPERATIONS IN MIPS32

Lecture 60: EXPLOITING INSTRUCTION LEVEL PARALLELISM

Lecture 61: VECTOR PROCESSORS

Lecture 62: MULTI-CORE PROCESSORS

Lecture 63: SOME CASE STUDIES

Lecture 64: SUMMARIZATION OF THE COURSE

Week 12 Lecture Material

Quiz: Week 12 : Assignment 12

Feedback form for Week 12

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2) Consider the given floating-point instruction:

L.D F2, 400(R6)

The data from location [R6+400] and [R6+404] will be loaded to which of the following registers?

- a. F1, F2
- b. F2, F3
- c. F3, F2
- d. None of these

- a.
- b.
- c.
- d.

1 point

3) Which of the following techniques can be used to improve the CPI?

- a. Sequencing unrelated instructions
- b. Separating related instructions
- c. Loop unrolling
- d. None of these

- a.
- b.
- c.
- d.

1 point

Assignments Solution

Live Interactive session

Text Transcripts

Books

4) Which of the following statement(s) is/are false for superscalar MIPS32 machine? 1 point

- a. It can issue multiple independent instructions every clock cycle.
- b. It can result in a CPI of less than 1.
- c. It can dynamically check dependency between instructions.
- d. It consists of more than one functional units that can run in parallel
- e. None of these.

- a.
- b.
- c.
- d.
- e.

5) Loop unrolling requires significantly greater number of registers? 1 point

- a. True
- b. False

- a.
- b.

6) Which of the following is/are advantage of vector processor? 1 point

- a. It gives good speedup when we carry out similar operations on vectors.
- b. No loop overhead.
- c. The number of instructions gets reduced.
- d. None of these.

- a.
- b.
- c.
- d.

7) In a vector processor, suppose that the start-up time of vector multiply operation is 20 clock cycles. After start-up, the initiation rate is 5 clock cycles. The number of clock cycles required per result for a 128-element vector will be _____

1 point

8) Which of the following statement(s) is/are false for various types of multi-core processors?

1 point

- a. In asymmetric multi-core system, all the cores are identical.
- b. In symmetric multi-core system, different cores may have different functionalities.
- c. In a tightly coupled multiprocessor all the processors have access to a common shared memory.
- d. None of these.

- a.
- b.
- c.
- d.

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your own answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.